IJIREEICE
ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526
International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering
nCORETech
LBS College of Engineering, Kasaragod
Vol. 3, Special Issue 1, February 2016

Seven Level Inverter Topologies: A Comparative Study

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Abstract: In the recent years, multilevel inverters (MLI) are highly being used for medium voltage and high power applications due to their various advantages such as low voltage stress on the power switches, low electromagnetic interferences (EMI), low dv/dt ratio to supply lower harmonic contents in the output voltage and current. Multilevel inverters have become more popular over the years in electric high power application with the promise of very low disturbances and the possibility to function at lower switching frequencies than ordinary two-level inverters. This paper presents different topologies, emphasizing mainly on seven level inverters. The different topologies compared are the diode-clamped inverter (neutral-point clamped), capacitor clamped (flying capacitor), and cascaded multi-cell with separate DC sources. Emerging topologies like asymmetric hybrid cells and soft-switched multilevel inverters are also discussed. Finally a seven level inverter topology with lesser number of switches is discussed and compared along with the other seven level inverter topologies. Simulation studies of diode clamped seven level inverter, cascade seven level inverter and seven level inverter with reduced number of switches are done. The seven level inverter with reduced number of switch with PWM (Pulse Width Modulation) switching is also simulated. It is observed that the pulse generation using PWM switching leads to further reduction of THD.

Keywords: Multilevel Converter, Multilevel inverter (MLI), Power converters, Total Harmonic Distortion.

I. INTRODUCTION

Inverter is a device which converts DC power into AC. The power in the battery is in DC mode and the motor that drives the wheels usually uses AC power, therefore there should be a conversion from DC to AC by a power converter, inverter is used for this conversion [1]. The two-level is the simplest topology used for this conversion that consists of four switches. Each switch needs an anti-parallel diode, so there should be also four anti-parallel diodes. There are many other topologies for inverters. A multilevel inverter (MLI) is a power electronic system that produces a sinusoidal voltage output from several DC sources. These DC sources can be fuel cells, solar cells, ultra capacitors, etc. The major function of multilevel inverters is to generate a better sinusoidal voltage and current in the output by using switches in series. Since many switches are put in series the switching angles are important in the multilevel inverters because all of the switches should be switched in such a way that the output voltage and current have low harmonic distortion (THD).

Comparing two-level inverter topologies of the same power ratings, MLIs also have the advantage that the harmonic components of line-to-line voltages fed to the load are reduced owing to its switching frequencies. The multilevel inverters have become increasingly attractive for researchers and manufacturers due to their advantages over conventional three-level pulse width modulated (PWM) inverters. The MLI produces improved output waveforms, low EMI, lower total harmonic distortion (THD) and reduced filter size. Multilevel inverter topology requires the least components for a given number of levels. Multilevel inverters can be classified into three types [2]. Diode clamped multilevel inverters [3]-[4], flying capacitor multilevel inverters [5] and cascaded H-bridge multilevel inverter [6]. The THD is decreased by increasing the number of levels. Though, an output voltage with low THD is desirable, increasing the number of levels leads to more hardware, also the control will be more complicated.

It is a tradeoff between price, weight, complexity and a very good output voltage with lower THD. Among these multilevel topologies the diode clamped inverters (DCMLI), particularly, the three-level structure has a wide popularity in motor drive applications besides other multi-level inverter topologies. But, it has got limitations such as complexity and number of clamping diodes for the DCMLIs, as the level exceeds. The Flying Capacitor Inverters (FCMLI) are based on balancing capacitors on phase buses and generate multilevel output voltage waveform clamped by capacitors instead of diodes. Cascaded H-Bridge MLI topology is based on the series connection of H-bridges with separate DC sources. Since the output terminals of the H bridges are connected in series, the DC sources must be isolated from each other. The need of several sources on the DC side of the inverter makes multilevel technology attractive for photo voltaic applications [6].

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The only drawback of the multilevel converter is that it requires a large amount of semiconductor switches. Lower voltage rated switches can also be used in the multilevel converter and as a result the active semiconductor cost is not considerably increased when compared with the two level cases.

On the other hand, each active semiconductor added requires associated gate drive circuitry and adds further complication to the converter mechanical layout. Another disadvantage is that small voltage steps are typically formed by isolated voltage sources or a bank of series capacitors. Isolated voltage sources may not always be readily available and series capacitors require voltage balance.

A multilevel converter can be implemented in different ways, each with advantages and disadvantages. The simplest techniques which involve the parallel or series connection of conventional converters is to form the multilevel waveforms. Complicated structures actually insert converters within converters.

Whatever approach is being chosen, the subsequent voltage or current rating of the multilevel converter will become a multiple of the individual switches, and therefore the power rating of the converter can exceed the limit imposed by the individual switching devices.

The paper is organized as follows: Different multi-level inverter topologies such as Diode-Clamped inverter, Capacitor-Clamped inverter, and Cascaded Multi cell inverter are discussed, initially for understanding the features of the multilevel inverters and the seven level inverter topology for each configurations is discussed. The comparative study of the seven level inverter of different topologies are studied.

II. INVERTER TOPOLOGIES

Many topologies, or circuit designs have evolved for creating high power AC from low voltage DC source. This section gives an introduction to the evaluation of different converter topologies which includes: Diode-Clamped Inverter (DCI), Capacitor-Clamped Inverter (CCI), Cascaded Multi-cell Inverters (CMI), Generalized Multilevel Cells (GMI) and Some Emerging Multilevel Inverter Topologies. These are briefly described below.

A. Diode-Clamped Inverter

This inverter is also called as Neutral-Point Clamped Inverter (NPC). In the NPCMLI topology the use of voltage clamping diodes is essential. A common DC-bus is divided by an even number of bulk capacitors in series with a neutral point in the middle of the line.

The number of capacitors depends on the number of voltage levels in the inverter. From this DC-bus, with neutral point and capacitors, there are clamping diodes connected to an (m-1) number of valve pairs, where m is the number of voltage levels in the inverter (voltage levels it can generate) [7].

A simple three-level diode-clamped inverter is shown in
Fig. 1(a). In this circuit, the DC-bus voltage is split into three levels by two series-connected bulk capacitors, C_1 and C_2. The middle point of the two capacitors 'n' can be defined as the neutral point. The output voltage v_{an} has three states: $V_{dc}/2$, 0, and $-V_{dc}/2$. For voltage level $V_{dc}/2$, switches S_1 and S_2 need to be turned on; for $-V_{dc}/2$, switches S_1' and S_2' need to be turned on; and for the 0 level, S_2 and S_1' need to be turned on. The key components that distinguish this circuit from a conventional two-level inverter are D_1 and D_1'.

These two diodes clamp the switch voltage to half the level of the DC-bus voltage. When both S_1 and S_2 turn on, the voltage across a and o is V_{dc}, i.e., $v_{a0} = V_{dc}$. In this case, D_1 balances out the voltage sharing between S_1'and S_2' with S_1' blocking the voltage across C_1 and S_2' blocking the voltage across C_2.

Therefore, the output voltage v_{an} is AC, and v_{a0} is DC. The difference between v_{an} and v_{a0} is the voltage across C_2, which is $V_{dc}/2$. If the output is taken out between a and o, then the circuit becomes a dc/dc converter, which has three output voltage levels: V_{dc}, $V_{dc}/2$ and 0.

Fig. 1(b) shows a seven-level diode-clamped converter in which the DC bus consists of six capacitors, C_1, C_2, C_3, C_4, C_5 and C_6. For DC-bus voltage V_{dc}, the voltage across each capacitor is $V_{dc}/6$, and each device voltage stress will be limited to one capacitor voltage level $V_{dc}/6$ through clamping diodes.

To explain how the staircase voltage is synthesized, the neutral point n is considered as the output phase voltage reference point.

There are seven switch combinations to synthesize seven level voltages across a and n is given in Table I.

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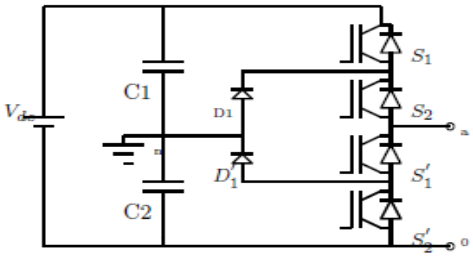
TABLE I: SWITCHING STATES FOR A SEVEN LEVEL DIODE CLAMPED INVERTER

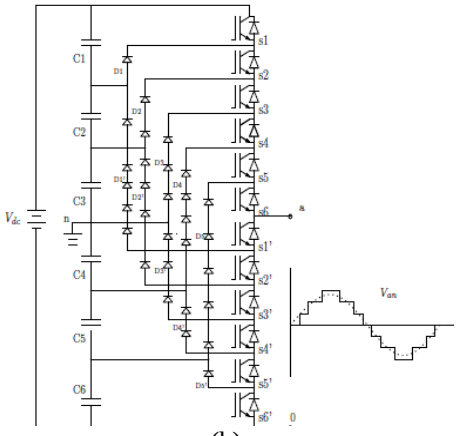
V_0	$V_{dc}/2$	$V_{dc}/3$	$V_{dc}/6$	0	$V_{dc}/6$	$V_{dc}/3$	$V_{dc}/2$
S_1	1	0	0	0	0	0	0
S_2	1	1	0	0	0	0	0
S_3	1	1	1	0	0	0	0
S_4	1	1	1	1	0	0	0
S_5	1	1	1	1	1	0	0
S_6	1	1	1	1	1	1	0
S_1'	0	1	1	1	1	1	1
S_2'	0	0	1	1	1	1	1
S_3'	0	0	0	1	1	1	1
S_4'	0	0	0	0	1	1	1
S_5'	0	0	0	0	0	1	1
S_6'	0	0	0	0	0	0	1

Six complementary switch pairs exist in each phase. The complementary switch pair is defined such that turning on one of the switches will exclude the other from being turned on. In this example, the six complementary pairs are (S_1; S_1'), (S_2; S_2'), (S_3; S_3'), (S_4 ; S_4'), (S_5 ; S_5') and (S_6; S_6').

Although each active switching device is only required to block a voltage level of V_{dc} /(m-1), the clamping diodes have different voltage ratings for reverse voltage blocking. Using D_1' of Fig. 1(b) as an example, when lower devices S_2'-S_6' are turned on, D_1' needs to block three capacitor voltages, or $3V_{dc}/4$. Similarly, D_3 and D_3' need to block $V_{dc}/2$, and D_4 needs to block $3V_{dc}/4$. Assuming that each blocking diode voltage rating is the same as the active device voltage rating, the number of diodes required for each phase will be (m-1) (m-2). This number represents a quadratic increase in m. When m is sufficiently high, the number of diodes required will make the system impractical to implement. If the inverter runs under PWM, the diode reverse recovery of these clamping diodes becomes the major design challenge in high-voltage high-power applications.



(a)



(b)

Fig. 1: Diode-clamped multilevel inverter circuit topologies
(a) Three-level (b) Seven-level

IJIREEICE
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ISSN (Print) 2321 – 5526
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The advantages and disadvantages of Diode Clamped Multilevel Inverter are [2]-[3]

Advantages:

- All of the phases share a common DC bus, which minimizes the capacitance requirements of the converter. For this reason, a back-to-back topology is not only possible but also practical for uses such as a high voltage back-to-back inter-connection or an adjustable speed drive.
- The capacitors can be pre-charged as a group.
- Efficiency is high for fundamental frequency switching.

Disadvantages:

- Real power flow is difficult for a single inverter because the intermediate DC levels will tend to overcharge or discharge without precise monitoring and control.
- Capacitor Voltage Balance problem that need complex modulation.
- The number of clamping diodes required is quadratically related to the number of levels, which can be cumbersome for units with a high number of levels.

B. Capacitor-Clamped Inverter

Capacitor Clamped (CC), or Flying Capacitor, topology is similar to the NPCMLI, topology. Instead of using clamping diodes it uses capacitors to hold the voltages to the desired values. As for the NPCMLI, m-1 number of capacitors on a shared DC-bus, where m is the level number of the inverter, and 2(m-1) switch-diode valve pairs are used. However, for the CCMLI, instead of clamping diodes, one or more (depending on position and level of the inverter) capacitors are used to create the output voltages. They are connected to the midpoints of two valve pairs on the same position on each side of the midpoint between the valves.

The inverter in Fig. 2(a) provides a three-level output across a and n, i.e., v_{an} = $V_{dc}/2$, 0, or $-V_{dc}/2$. For voltage level $V_{dc}/2$, switches S_1 and S_2 need to be turned on; for $-V_{dc}/2$, switches S_1' and S_2' need to be turned on; and for the 0 level, either pair (S_1; S_1') or (S_2; S_2') need to be turned on. Clamping capacitor C_1 is charged when S_1 and S_1' are turned on, and is discharged when S_2 and S_2' are turned on. The charge of C_1 can be balanced by proper selection of the 0-level switch combination.

The voltage synthesis in a seven-level capacitor-clamped converter has more flexibility than a diode-clamped converter. Using Fig. 2(b) as the example, the voltage of the seven-level phase-leg a output with respect to the neutral point n, v_{an}, can be synthesized by the switch combinations as given in Table II.

TABLE II: SWITCHING STATES FOR A SEVEN LEVEL CAPACITOR CLAMPED INVERTER

V_0	$V_{dc}/2$	$V_{dc}/3$	$V_{dc}/6$	0	$V_{dc}/6$	$V_{dc}/3$	$V_{dc}/2$
S_1	1	1	1	1	1	1	0
S_2	1	1	1	1	1	0	0
S_3	1	1	1	1	0	0	0
S_4	1	1	1	0	0	0	0
S_5	1	1	0	0	0	0	0
S_6	1	0	0	0	0	0	0
S_1'	0	1	1	1	1	1	1
S_2'	0	0	1	1	1	1	1
S_3'	0	0	0	1	1	1	1
S_4'	0	0	0	0	1	1	1
S_5'	0	0	0	0	0	1	1
S_6'	0	0	0	0	0	0	1

Similar to diode clamping, the capacitor clamping requires a large number of bulk capacitors to clamp the voltage. Provided that the voltage rating of each capacitor used is the same as that of the main power switch, an m-level converter will require a total of (m-1)(m-2)/2 clamping capacitors per phase leg in addition to (m-1) main DC-bus capacitors. The advantages and disadvantages of capacitor clamped inverters are given below [2] - [3].

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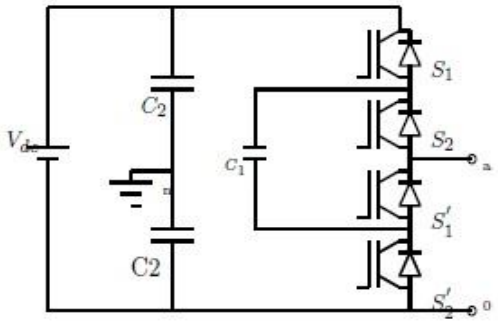
Advantages:

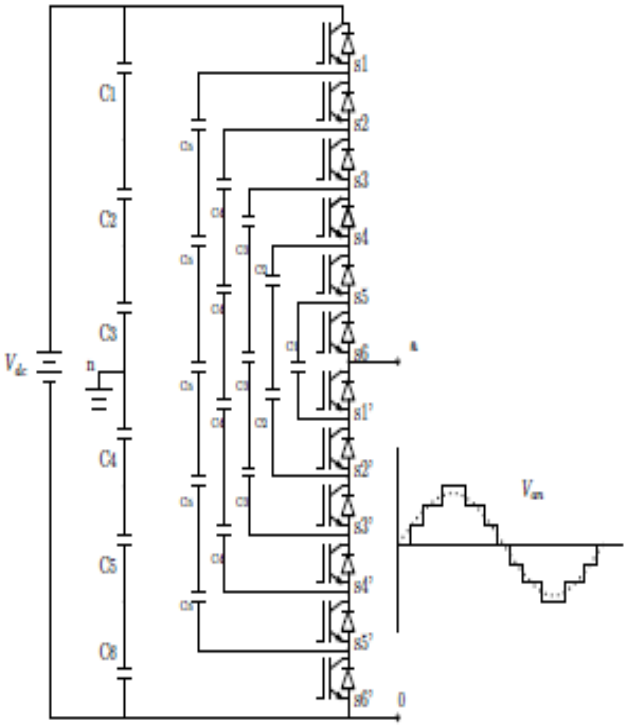
- Phase redundancies are available for balancing the voltage levels of the capacitors.
- Real and reactive power flow can be controlled.
- The large number of capacitors enables the inverter to ride through short duration outages and deep voltage sags.

Disadvantages:

- Control is complicated to track the voltage levels for all of the capacitors. Also, pre charging all of the capacitors to the same voltage level and startup are complex.
- Switching utilization and efficiency are poor for real power transmission.
- The large numbers of capacitors are both more expensive and bulky than clamping diodes in multilevel diode-clamped converters. Packaging is also more difficult in inverters with a high number of levels.
- Complicated control, leading to high switching frequency and losses, when transferring real power.



(a)



(b)

Fig. 2: Capacitor-clamped multilevel inverter circuit topologies (a)Three-level (b)Seven-level

C. Cascaded Multi cell Inverters

A cascaded multilevel inverter consists of a series of single phase full bridge inverter units. Each separate DC source is connected to a full bridge inverter. The cascaded multilevel inverter does not require any voltage clamping diodes or voltage balancing capacitors like other two topologies.

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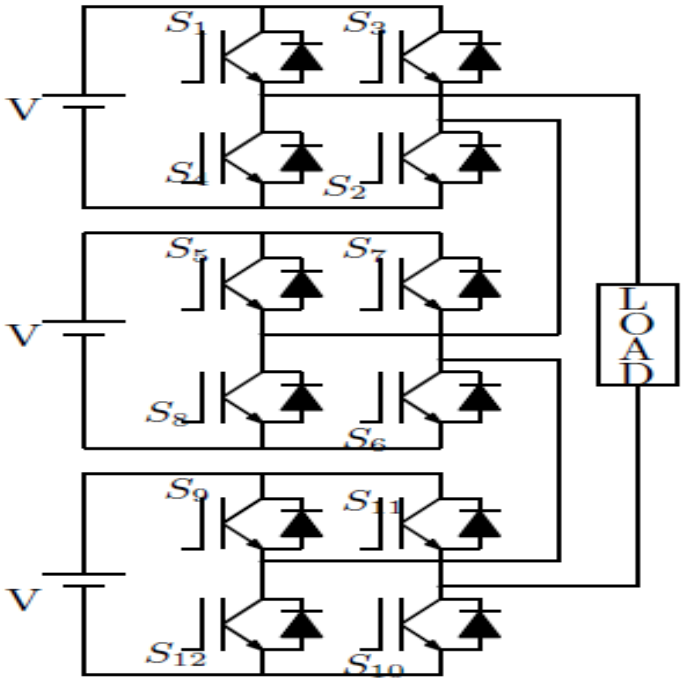
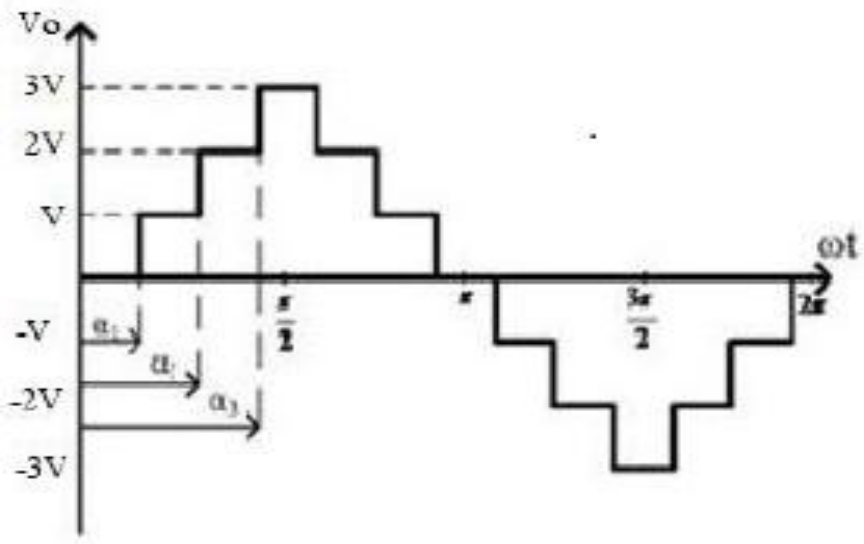
The seven-level multilevel inverter is obtained by cascading three full bridge inverter circuits. The three full bridge inverters are connected in series and a single phase output is taken. Each full bridge is fed from separate DC source. The number of output levels m in each phase is related to number of full bridge inverter units n by, m/2n+1. Here number of levels is seven, hence number of inverter circuits connected in series is three. The single phase seven-level topology of cascaded H bridge multilevel inverter is shown in Fig. 3(a).

Each H-bridge is fed with the same value of DC voltage hence it can be called as symmetrical cascaded multilevel inverter. Each full bridge inverter can generate three different voltage outputs: $+V_{dc}$, 0, and $-V_{dc}$. The output voltage is synthesized by sum of three inverter outputs are at three angles. These three angles are used for giving pulses to twelve switches. The switching pattern for single phase seven-level topology of cascaded H-bridge multilevel inverter is shown in Table III. The advantages and disadvantages are summarized below [2] - [8].



(a)



(b)

Fig. 3: Cascade inverter circuit topology
(a) Seven-level (b) Output waveform

IJIREEICE
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Vol. 3, Special Issue 1, February 2016

TABLE III: SWITCHING STATES FOR A SEVEN LEVEL CASCADE INVERTER

V_0	+V	+2V	+3V	0	-V	-2V	-3V
S_1	1	1	1	0	0	0	0
S_2	1	1	1	1	0	0	0
S_3	0	0	0	0	1	1	1
S_4	0	0	0	1	1	1	1
S_5	0	1	1	0	0	0	0
S_6	1	1	1	1	1	0	0
S_7	0	0	0	0	0	1	1
S_8	1	0	0	1	1	1	1
S_9	0	0	1	0	0	0	0
S_{10}	1	1	1	1	1	1	0
S_{11}	0	0	0	0	0	0	1
S_{12}	1	1	0	1	1	0	1

Advantages:

- The number of possible output voltage levels is more than twice the number of DC sources (m = 2s + 1).
- The series of H-bridges makes for modularized layout and packaging. This will enable the manufacturing process to be done more quickly and cheaply.
- Possibility to implement soft-switching.
- Simple voltage balancing modulation.

Disadvantages:

- Separate DC sources are required for each of the H bridges. This will limit its application to products that already have multiple SDCSs readily available.
- No common DC-bus.

D. Generalized Multilevel Cells

The existing multilevel inverters such as diode-clamped and capacitor-clamped multilevel inverters can be derived from the generalized inverter topology. Moreover, the generalized multilevel inverter topology can balance each voltage level by itself regardless of load characteristics. Therefore, the generalized multilevel inverter topology provides a true multilevel structure that can balance each DC voltage level automatically at any number of levels, regardless of active or reactive power conversion, and without any assistance from other circuits. Thus, in principle, it provides a complete multilevel topology that embraces the existing multilevel inverters.

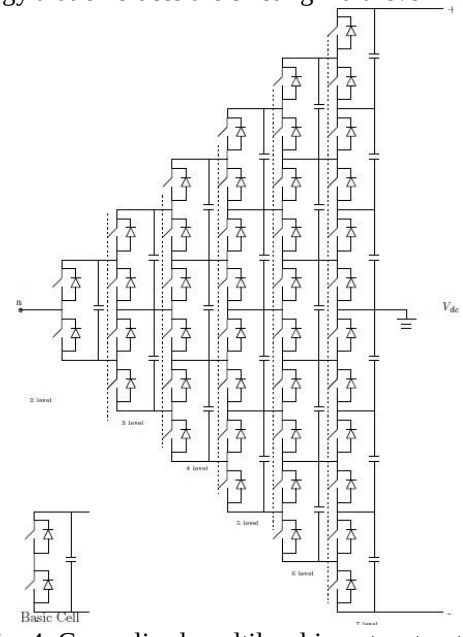

Fig. 4: Generalized multilevel inverter structure

IJIREEICE
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Fig. 4 shows the multilevel inverter structure per phase leg. Each switching device, diode, or capacitors voltage is V_{dc}, i.e., 1/(1 - m) of the DC-link voltage. Any inverter with any number of levels, including the conventional two-level inverter can be obtained using this generalized topology.

E. Modified Multilevel Inverter Topologies

1. Mixed-Level Hybrid Multilevel Cells:

For high voltage high-power applications, it is possible to adopt multilevel diode-clamped or capacitor-clamped inverters to replace the full-bridge cell in a cascaded inverter. The reason for doing so is to reduce the number of separate DC sources.

The seven-level cascaded inverter shown in Fig 3 requires three separate DC sources for one phase leg and nine for a three-phase inverter. If a three-level inverter replaces the full-bridge cell, the voltage level is effectively doubled for each cell. Thus, to achieve the nine voltage levels for each phase, only two separate DC sources are needed for one phase leg and six for a three-phase inverter. The configuration can be considered as having mixed-level hybrid multilevel cells because it embeds multilevel cells as the building block of the cascaded inverter. Fig. 5 shows the nine-level cascaded inverter incorporating a three-level capacitor-clamped inverter as the cell. It is obvious that a diode-clamped inverter can replace the capacitor-clamped inverter to be a mixed-level hybrid multilevel cell.

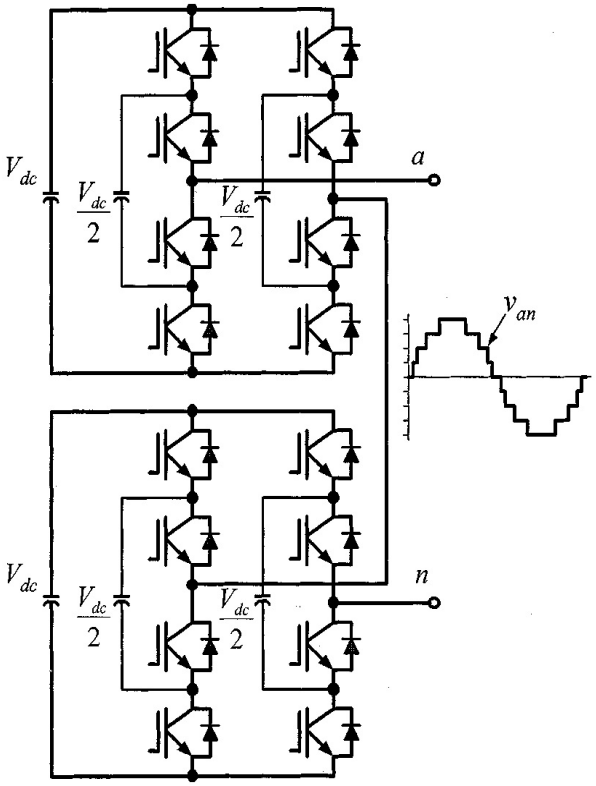

Fig. 5: A mixed-level hybrid cell configuration using the three level diode-clamped inverter as the cascaded inverter cell to increase the voltage levels.

1. Asymmetric Hybrid Multilevel Cells:

In Mixed Level Hybrid multilevel structure, the voltage levels of the cascade inverter cells equal each other. However, it is possible to have different voltage levels among the cells and the circuit can be called as asymmetric hybrid multilevel inverter.

Fig. 6 shows an example of having three separate DC-bus levels, one with V_{dc}, and the others with $V_{dc}/2$ and $V_{dc}/4$. Depending on the availability of DC sources, the voltage levels are not limited to a specific ratio. This feature allows more levels to be created in the output voltage, and thus reduces the harmonic contents with less cascaded cells required [8].

Even with the same voltage level among them, it is also possible to use high-frequency PWM for one cell, while the other switches at a lower rate.

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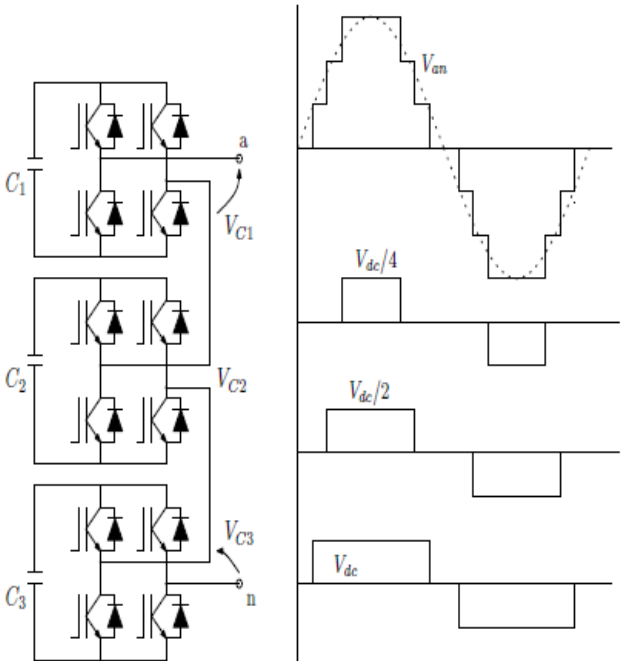

Fig. 6: Asymmetric hybrid cascaded inverter cell arrangement with different voltage levels

2. Soft-Switched Multilevel Inverters:

There are numerous ways of implementing soft-switching methods to reduce the switching loss and to increase efficiency for different multilevel inverters. For the cascaded inverter, because each inverter cell is a two-level circuit, the implementation of soft switching is not at all different from that of conventional two-level inverters. For capacitor-clamped or diode-clamped inverters, however, the choices of soft-switching circuit can be found with different circuit combinations.

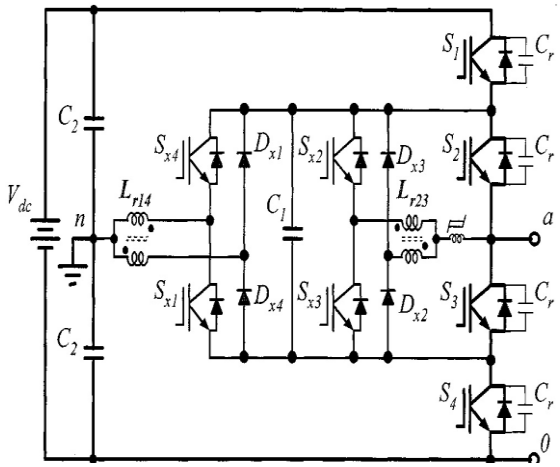

Fig. 7: Zero-voltage switching capacitor clamped inverter circuit

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Although zero-current switching is possible, most literatures propose zero-voltage-switching types including auxiliary resonant commutated pole (ARCP), coupled inductor with zero-voltage transition (ZVT), and their combinations. Fig. 7 shows an example of combining the ARCP and coupled-inductor ZVT techniques for a capacitor clamped three-level inverter.

The auxiliary switches S_{x2}, S_{x3}, D_{x2}, and D_{x3} are used to assist the inner main switches S_2 and S_3 to achieve soft switching. With L_{r23} as the coupled inductor, the bridge-type circuit formed by S_{x2}, S_{x3}, S_2, and S_3 forms a two-level coupled-inductor ZVT. The basic principle of a two-level ZVT can be found in. For the outer main switches, the soft switching relies on S_1 and S_4, S_{x1}, S_{x4}, D_{x1}, D_{x4}, coupled inductor L_{r14}, and split-capacitor pair C_2 to form an ARCP type soft switching inverter.

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F. Seven Level Inverter with reduced number of switches

As seen in Fig. 8, the seven-level inverter is composed of a capacitor selection circuit and a full-bridge power converter, which are connected in cascade [9]. The operation of the seven level inverter can be divided into the positive half cycle and the negative half cycle of the utility. For ease of analysis, the power electronic switches and diodes are assumed to be ideal, while the voltages of both capacitors C_1 and C_2 in the capacitor selection circuit are constant and equal to $V_{dc}/3$ and $2V_{dc}/3$, respectively. The operation of the seven-level inverter in the positive half cycle of the utility can be further divided into four modes, as shown in Table IV

In the negative half cycle, the output current of the seven level inverter is negative. The operation of the seven-level inverter can also be further divided into four modes, as shown in Table V. Advantages of the seven level inverter with reduced number of switches is briefed below.

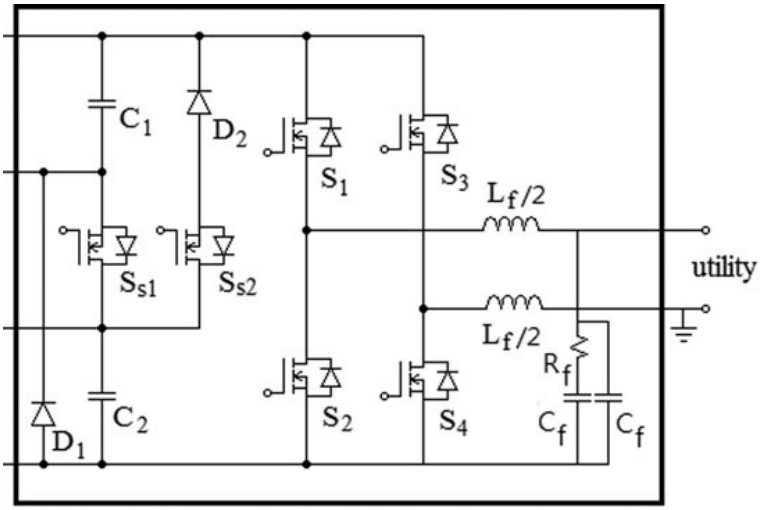

Fig. 8: Seven level inverter with reduced number of switches

Advantages:

- This seven level inverter contains only six power electronics switches, which simplifies the circuit configuration.
- Reduced switching power loss, because only one power electronic switch is switched at high frequency at any time to generate the 7 level output voltage.

G. Comparison of Multi Level Inverters

Comparison of multilevel inverter is made based on the following criteria's:

- Number of semiconductor devices used per phase leg.
- Number of DC bus capacitors used.
- Number of balancing capacitors used per phase leg.
- Amplitude of fundamental and dominant harmonic components.
- Total Harmonic Distortion of output voltage.
- Control complexity based on voltage unbalances and power switches.
- Cost estimation in fabrication of power circuit and the associated components.

In high power systems, the multilevel inverters can appropriately replace the existing system that use traditional multi-pulse converters without the need for transformers. All three multilevel inverters can be used in reactive power compensation without having the voltage unbalance problem.

Table. VI compares the power component requirements per phase leg among the three multilevel voltage source inverters mentioned above.

Clamping diodes were not needed in flying-capacitor and cascaded-inverter configuration, while balancing capacitors were not needed in diode clamp and cascaded-inverter configuration.

Implicitly, the multilevel converter using cascaded-inverters requires the least number of components.

IJIREEICE
ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526
International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering
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TABLE VI: Comparison of different multilevel inverter topologies

Topology	Diode Clamped	Capacitor Clamped	Cascaded
Power semiconductor Switches	2(m-1)	2(m-1)	2(m-1)
Clamping diodes per Phase	(m-1)(m-2)	0	0
DC bus capacitor	(m-1)	(m-1)	(m-1)/2
Balancing capacitor per Phase	0	(m-1)(m-2)/2	0
Voltage unbalancing	Average	High	Very small

H. Comparison of Seven Level Inverters

Four different topologies of seven level inverters are discussed here. These are Diode clamped seven level inverter, Capacitor clamped seven level inverter, Cascade seven level inverter and Seven level inverter with reduced number of switches.

TABLE VII: Comparison of Seven level inverter topologies

Topology	Power semi-conductor switches	Clamping diodes per phase	DC bus capacitor	Balancing capacitor per phase
Seven level Diode Clamped	12	30	6	0
Seven level Capacitor Clamped	12	0	6	15
Seven level Cascaded	12	0	3	0
Seven level topology with reduced number of switches	6	0	2	0

Table VII shows that number of switches and diodes required to generate seven level output voltage by the new topology is far lesser than that required by the other conventional MLI topologies.

III. SIMULATION AND RESULTS

Simulation study of different seven level inverter topologies such as seven level diode clamped inverter, seven level cascade inverter and seven level inverter with reduced number of switches are discussed here. The THD levels of voltages and currents are measured.

A. Cascade seven level inverter

The Fig.9 shows the simulation diagram of seven level cascade inverter. The output waveform is shown in Fig.10 and the THD profile of the output waveform of cascade seven level inverter is shown in Fig .11. THD observed was 33.59%.

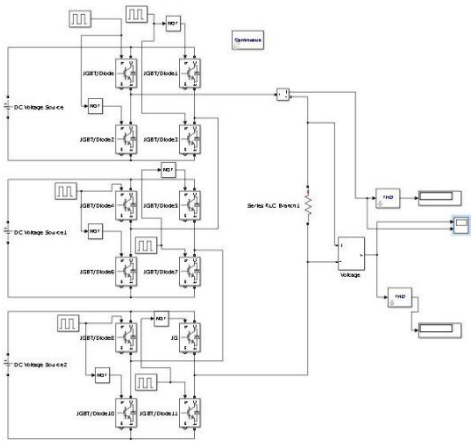

Fig. 9: Simulation diagram of Cascade Seven level inverter

IJIREEICE
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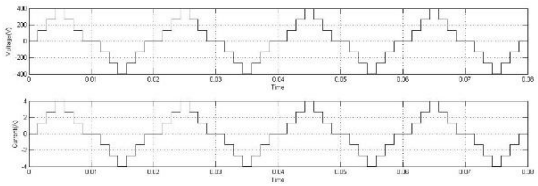

Fig. 10: Output Waveforms of seven level cascade inverter

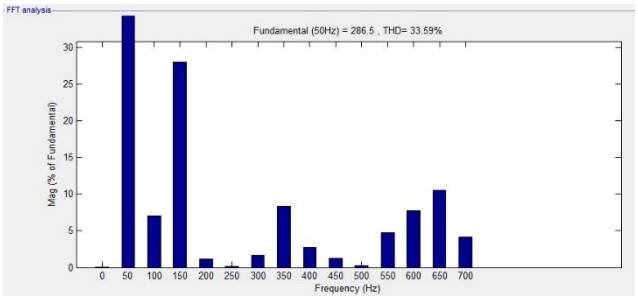

Fig. 11: THD profile of seven level cascade inverter output voltage

B. Diode Clamped Seven level inverter

Diode Clamped seven level inverter has 12 switches, 30 Clamping diodes and 6 DC bus capacitors in its configuration. Fig.12 shows the simulation diagram of seven level diode clamped inverter, and the output waveform is shown in Fig.13. The seven level output waveform is shown in Fig.13. And the THD of this output waveform is obtained from Fig.14 and is 31.35%.

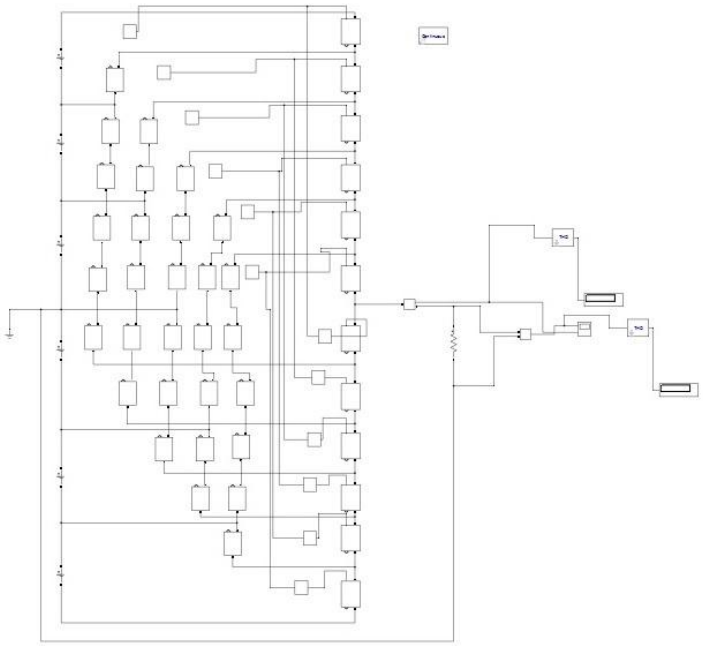

Fig. 12: Simulation diagram of Diode clamped Seven level inverter

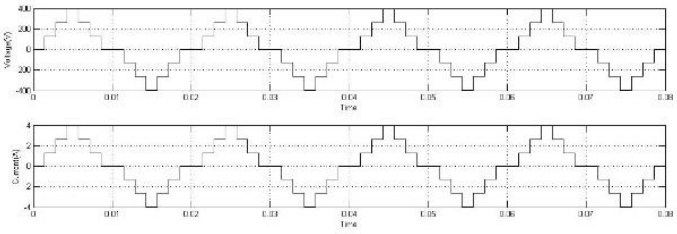

Fig. 13: Output Waveforms of seven level diode clamped Inverter

IJIREEICE
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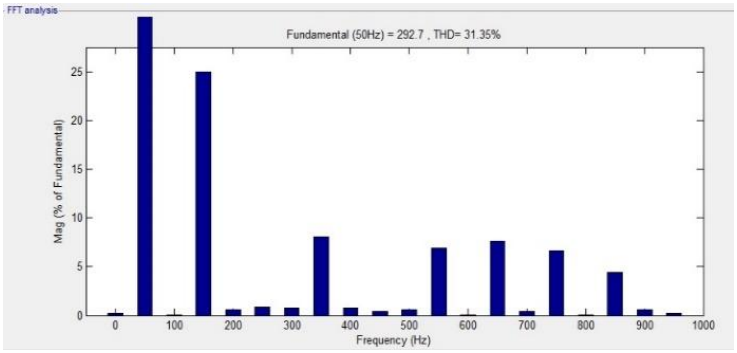

Fig. 14: THD value of output voltage of seven level diode clamped inverter

C. Seven level inverter with reduced number of switches

This is a seven level inverter which contains only six power electronics switches.

Fig. 15 shows the simulation diagram of seven level inverter with reduced number of switches, and the output waveform is shown in Fig.16.The THD of the output waveform is obtained from Fig.17 and is 31.47%.

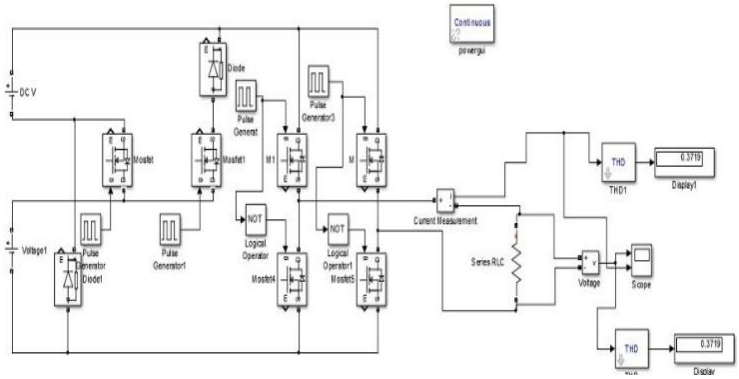

Fig. 15: Simulation diagram of Seven level inverter with reduced number of switches

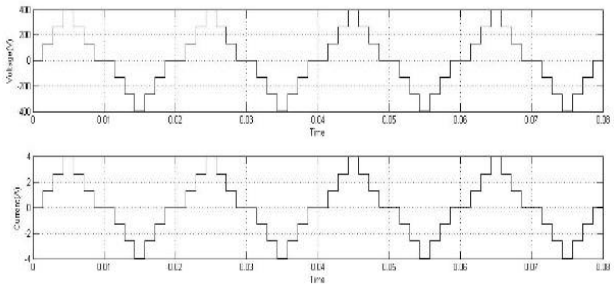

Fig. 16: Output Waveforms of seven level inverter with reduced number of switches

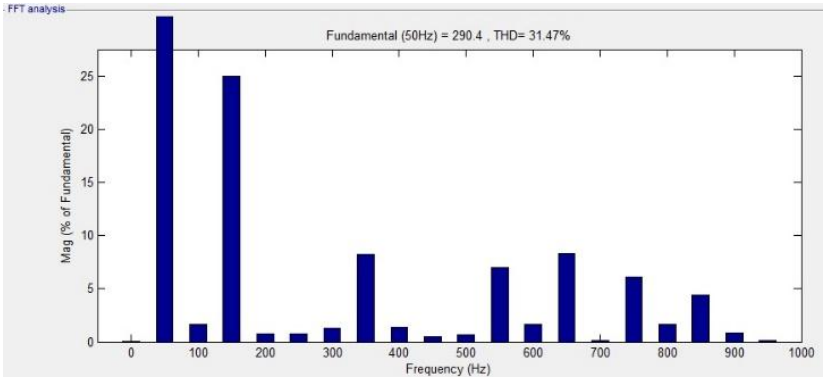

Fig. 17: THD value of output voltage of seven level inverter With reduced number of switches

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D. THD Comparison of seven level inverters

The THDs of three topologies compared. The THDs of output voltage and output current are measured.

TABLE VIII: THD Comparison

Topology	Seven level Diode clamped inverter	Seven level cascade inverter	Seven level inverter with reduced number of switches
Voltage THD %	31.35	33.59	31.47
Current THD %	31.35	33.59	31.47

The table shows that the lowest THD is for Cascade seven level inverters. The THD of seven level inverter with reduced number of switch is compatible with that of the seven level cascade inverter. The advantage of seven level inverter with reduced number of switch is as in the number of switches as given by Table VII.

E. Seven level inverter with PWM switching

In all the above simulations the pulse is generated using pulse generators. In this pulse width modulation (PWM) is used to generate the control signals for the six power electronics switches. Fig.18 shows the simulation diagram of seven level inverter with PWM switching. And the output waveform is shown in Fig.19. From this simulation we get the seven level output which is shown in Fig.19. The THD of the output waveform is obtained from Fig.20. The THD is reduced to 12.97%.

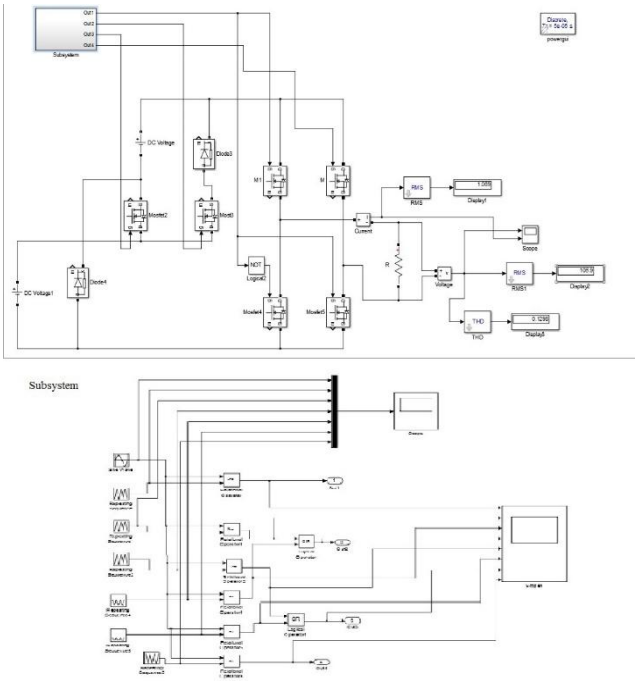

Fig. 18: Simulation diagram of seven level inverter with PWM switching

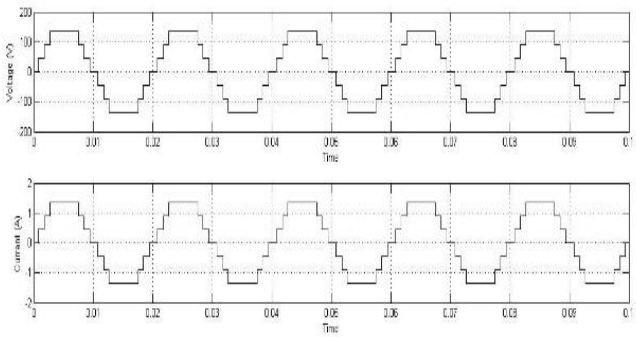

Fig. 19: Output Waveforms of seven level inverter with PWM Switching

IJIREEICE

ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

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Vol. 3, Special Issue 1, February 2016

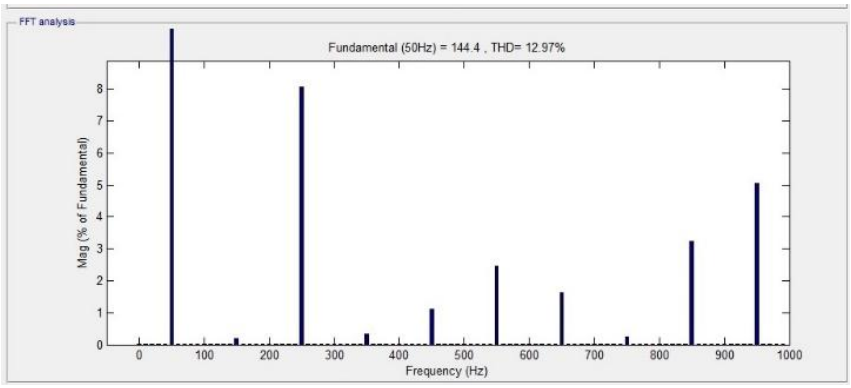

Fig. 20: THD value of output voltage of seven level inverter with PWM switching

IV. CONCLUSION

This paper has provided a brief summary and comparison of different multilevel inverter circuit topologies. The THD with respect to the number of switches is compared in this paper. Simulation results of three seven level inverter topologies are discussed. The THD of Cascade seven level inverter and Seven level inverter with reduced number of switches are higher than that of Diode clamped seven level inverter and THD of seven level inverter with reduced number of switches is comparable with that of the seven level Diode clamped inverter. The THD present in the output voltage of DCI is 31.35% and cascade inverter is 33.59% and that for seven level inverter with reduced number of switch is 31.47%. Simulation study shows that by using pulse width modulation (PWM) for pulse generation the THD can be further reduced. The THD is reduced to 12.97%. The Seven level Diode clamped inverter and Cascade multilevel inverter has 12 switches in its topology and the other topology contain only 6 switches. Therefore switching losses are reduced. Multilevel inverters can be used instead of two level inverters to get lower THD in both output voltage and current and also to lower the switching power losses.

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